AMENDMENTS TO THE CLAIMS

Claims 1-14 (Cancelled)

15. (Currently Amended) A method of forming a plurality of semiconductor ~~circuit~~ devices in a semiconductor material having a first semiconductor region of a first conductivity type, a second semiconductor region of a second conductivity type, and a third semiconductor region of the second conductivity type, the method comprising ~~the steps of~~:

~~implanting a first dopant into~~ simultaneously doping the first semiconductor region and the second semiconductor region while protecting the third semiconductor region from being doped; and

~~implanting a second dopant into~~ simultaneously doping the second semiconductor region and the third semiconductor region while protecting the first semiconductor region from being doped.

16. (Currently Amended) The method of claim 15 and further comprising ~~the steps of~~:

forming a layer of first oxide on the first semiconductor region;

forming a layer of second oxide on the second semiconductor region and the third semiconductor region, a thickness of the layer of first oxide being greater than a thickness of the layer of second oxide.

17. (Currently Amended) The method of claim 16 and further comprising ~~the steps of~~:

forming spaced-apart first source and drain regions of the second conductivity type in the first semiconductor region;

forming spaced-apart second source and drain regions of the first conductivity type in the second semiconductor region; and

forming spaced-apart third source and drain regions of the first conductivity type in the third semiconductor region.

18. (Currently Amended) The method of claim 17 wherein:

the semiconductor material further includes a fourth semiconductor region of the first conductivity type, and

~~the second implanting step includes the steps of:~~

~~implanting a dopant into the second region and the third region; and~~

~~implanting a dopant into the second region, the third region, and the fourth region~~

the fourth semiconductor region is doped when the second and third semiconductor regions are simultaneously doped before the second and third source and drain regions are formed.

19. (Currently Amended) The method of claim 18 and further comprising ~~the step of~~ forming spaced-apart fourth source and drain regions of the second conductivity type in the fourth semiconductor region.

Claims 20-22 (Cancelled)

23. (Currently Amended) The method of claim 16 and further comprising ~~the steps of~~:

forming a layer of polysilicon on the layer of second oxide; and

etching the layer of polysilicon to form a first gate over the second semiconductor region and a second gate over the third semiconductor region, the first gate having a length that is 0.3-0.8 as long as a length of the second gate.

24. (Currently Amended) The method of claim 16 wherein:

the semiconductor material further includes a fourth semiconductor region of the first conductivity type,

the fourth semiconductor region is ~~implanted~~ doped when the first semiconductor region is ~~implanted~~ doped;

the layer of first gate oxide lies over a portion of the fourth semiconductor region; and

a layer of third gate oxide lies over a portion of the fourth semiconductor region, the layer of third gate oxide being thinner than the layer of first gate oxide.

25. (Cancelled)

26. (Currently Amended) The method of claim 16 wherein:

the semiconductor material further includes a fourth semiconductor region of the first conductivity type; and

the fourth semiconductor region is ~~implanted~~ doped when the second semiconductor region and the third semiconductor region are ~~implanted at a same time~~ simultaneously doped before source and drain regions are formed in the second and third semiconductor regions.

27. (New) The method of claim 15 and further comprising:

forming spaced-apart first source and drain regions of the second conductivity type in the first semiconductor region; and

forming spaced-apart second source and drain regions of the first conductivity type in the second semiconductor region, and spaced-apart third source and drain regions of the first conductivity type in the third semiconductor region.

28. (New) A method of forming a plurality of semiconductor devices in a semiconductor material having a first semiconductor region of a first conductivity type, a second semiconductor region of a second conductivity type, and a third semiconductor region of the second conductivity type, the first, second, and third semiconductor regions being spaced apart and each having a channel region, the method comprising:

simultaneously doping the channel region of the first semiconductor region and the channel region of the second semiconductor region to define a threshold voltage in the channel region of the first semiconductor region, and partially define a threshold voltage in the channel region of the second semiconductor region;

simultaneously doping the channel region of the second semiconductor region and the channel region of the third semiconductor region to partially define the threshold voltage in the channel region of the second semiconductor region, and partially define a threshold voltage in the channel region of the third semiconductor region; and

simultaneously doping the channel region of the second semiconductor region and the channel region of the third semiconductor region to define the threshold voltage in the channel region of the second semiconductor region, and define the threshold voltage in the channel region of the third semiconductor region.

29. (New) The method of claim 28 and further comprising:

doping the first semiconductor region to form a first source region and a first drain region that define a first channel length measured along a shortest path from the first source region to the first drain region; and

simultaneously doping the second and third semiconductor regions to form a second source region and a second drain region that define a second channel length measured along a shortest path from the second source region to the second drain region, and a third source region and a third drain region that define a third channel length measured along a shortest path from the third source region to the third drain region.

30. (New) The method of claim 29 wherein the second channel length is shorter than the third channel length.

31. (New) The method of claim 30 wherein the first channel length is longer than the third channel length.

32. (New) The method of claim 28 and further comprising:

forming a layer of first oxide on the first semiconductor region;

forming a layer of second oxide on the second semiconductor region and the third semiconductor region, a thickness of the layer of first oxide being greater than a thickness of the layer of second oxide.

33. (New) The method of claim 32 and further comprising forming a first gate, a second gate, and a third gate, the first gate contacting the layer of first oxide over the first semiconductor region, the second gate contacting the layer of second oxide over the second semiconductor region, and the third gate contacting the layer of second oxide over the third semiconductor region, the second gate being shorter than the third gate.

34. (New) The method of claim 33 wherein the first gate is longer than the third gate.

35. (New) The method of claim 33 and further comprising:

doping the first semiconductor region to form a first source region and a first drain region that define a first channel length measured along a shortest path from the first source region to the first drain region; and

simultaneously doping the second and third semiconductor regions to form a second source region and a second drain region that define a second channel length measured along a shortest path from the second source region to the second drain region, and a third source region and a third drain region that define a third channel length measured along a shortest path from the third source region to the third drain region.

36. (New) The method of claim 35 wherein:

the second channel length is shorter than the third channel length; and

the first channel length is longer than the third channel length.

37. (New) The method of claim 35 wherein:

more than a leakage current flows between the second source region and the second drain region when the second gate, the second source region, and the second semiconductor region are connected to a same potential; and

substantially no current flows between the third source region and the third drain region when the third gate, the third source region, and the third semiconductor region are connected to a same potential.

38. (New) The method of claim 28 wherein:

the semiconductor material further includes a fourth semiconductor region of the first conductivity type, the fourth semiconductor region having a channel region;

the channel region of the fourth semiconductor region is doped to partially define the threshold voltage in the channel region of the fourth semiconductor region when the second and third semiconductor regions are doped to partially define the threshold voltages in the channel regions of the second and third semiconductor regions; and

the channel region of the fourth semiconductor region is doped to define the threshold voltage in the channel region of the fourth semiconductor region when the second and third semiconductor regions are doped to define the threshold voltages in the channel regions of the second and third semiconductor regions.